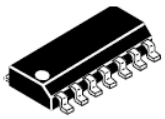
# Dual high-speed CAN transceiver

The CM0902 is a SMARTMOS dual high-speed (up to 1.0 Mbit/s) CAN transceiver device, providing the physical interface between the CAN protocol controller of an MCU and the physical dual wire CAN bus. Both channels are completely independent, featuring CAN bus wake-up on each CAN interface, and TXD dominant timeout functionality (33CM0902 only).

The CM0902 is packaged in a 14-pin SOIC, with industry standard pin out, and offers excellent EMC and ESD performance without the need for external filter components.The CM0902 comes in two variants: 33CM0902 and 34CM0902 for Automotive and Industrial applications respectively.

**CM0902**

**CAN HIGH-SPEED TRANSCEIVER**



**EF SUFFIX (PB-FREE)**
**98ASB42565B**
**14-PIN SOICN**

### Features

- Very low-current consumption in standby mode
- Compatible with +3.3 V or +5.0 V MCU interface
- Standby mode with remote CAN wake-up
- Pin and function compatible with market standard

Cost efficient robustness:

- High system level ESD performance
- Very high electromagnetic immunity and low electromagnetic emission without common mode choke or other external components.

Fail-safe behaviors:

- TXD Dominant timeout (33CM0902 only)
- Ideal passive behavior when unpowered, CAN bus leakage current <10 µA.
- $V_{DD}$ and $V_{IO}$ monitoring

### Automotive applications (33CM0902)

- Supports automotive CAN high-speed applications
- Body electronics
- Power train
- Chassis and safety
- Infotainment
- Diagnostic equipment
- Accessories

### Industrial applications (34CM0902)

- Transportation
- Backplanes
- Lift/elevators
- Factory automation
- Industrial process control

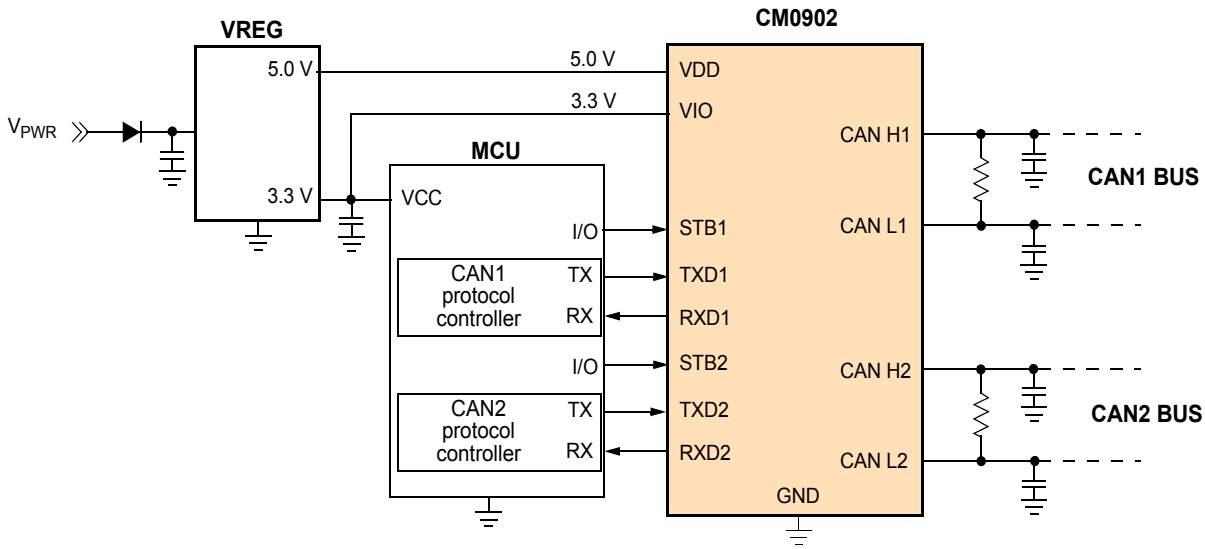



**Figure 1. Simplified application diagram**

* This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

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# 1 Orderable parts

This section describes the part numbers available to be purchased along with their differences.

**Table 1. Orderable part variations**

| Part number [1] | Temperature ($T_A$) | Package | TXD dominant protection |
|---|---|---|---|
| MC33CM0902WEF | -40 °C to 125 °C | SOIC 14 pins | Available |
| MC34CM0902WEF | -40 °C to 85 °C | | Not Available |

Notes
1. To Order parts in Tape & Reel, add the R2 suffix to the part number.

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to http://www.nxp.com and perform a part number search.

# 2 Internal block diagram

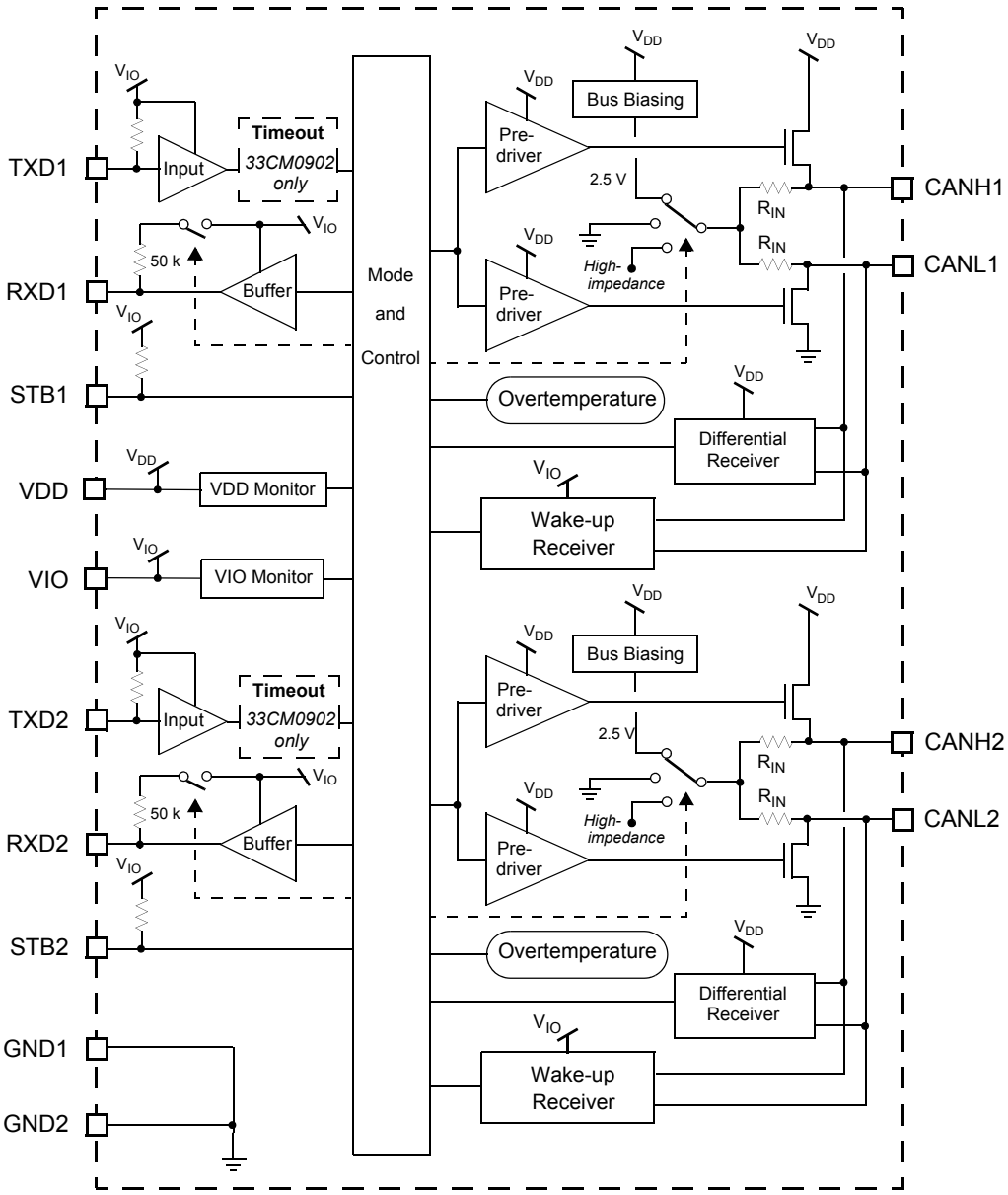



**Figure 2. Internal block diagram**

# 3 Pin connections

## 3.1 Pinout

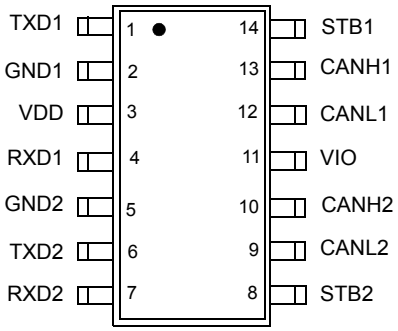



**Figure 1. 14-Pin SOIC pinout**

## 3.2 Pin definitions

A functional description of each pin can be found in the Functional Pin Description section beginning on page 14.

**Table 2. CM0902 pin definitions**

| Pin number | Pin name | Pin function | Definition |
|---|---|---|---|
| 1 | TXD1 | Input | CAN1 bus transmit data pin |
| 2 | GND1 | Ground | Ground 1 |
| 3 | VDD | Input | 5.0 V input supply for CAN driver and receiver |
| 4 | RXD1 | Output | CAN1 bus receive data pin |
| 5 | GND2 | Ground | Ground 2 |
| 6 | TXD2 | Input | CAN2 bus transmit data pin |
| 7 | RXD2 | Output | CAN2 bus receive data pin |
| 8 | STB2 | Input | Standby input for CAN2 mode selection |
| 9 | CANL2 | Input/Output | CAN2 low pin |
| 10 | CANH2 | Input/Output | CAN2 high pin |
| 11 | VIO | Input | Input supply for the digital input output pins |
| 12 | CAN L1 | Input/Output | CAN1 low pin |
| 13 | CAN H1 | Input/Output | CAN1 high pin |
| 14 | STB1 | Input | Standby input for CAN1 mode selection |

# 4 General product characteristics

## 4.1 Maximum ratings

**Table 3. Maximum ratings**

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

| Symbol | Description (rating) | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| **Electrical ratings** | | | | | |
| $V_{DD}$ | $V_{DD}$ Logic Supply Voltage | | 7.0 | V | |
| $V_{IO}$ | Input/Output Logic Voltage | | 7.0 | V | |
| $V_{STB1}$<br>$V_{STB2}$ | Standby pin Input Voltage | | 7.0 | V | |
| $V_{TXD1}$<br>$V_{TXD2}$ | TXD Maximum Voltage Range | | 7.0 | V | |
| $V_{RXD1}$<br>$V_{RXD2}$ | RXD Maximum Voltage Range | | 7.0 | V | |
| $V_{CANH1}$<br>$V_{CANH2}$ | CANH Bus Pin Maximum Range | -40 | 40 | V | |
| $V_{CANL1}$<br>$V_{CANL2}$ | CANL Bus Pin Maximum Range | -40 | 40 | V | |
| $V_{ESD}$ | ESD Voltage<br>• Human Body Model (HBM) (all pins except CANHx and CANLx pins)<br>• Human Body Model (HBM) (CANHx, CANLx pins)<br>• Machine Model (MM)<br>• Charge Device Model (CDM) (corner pins)<br>• System level ESD<br>• 330 Ω / 150 pF unpowered according to IEC61000-4-2:<br>• 330 Ω / 150 pF unpowered according to OEM LIN, CAN, FLexray Conformance<br>• 2.0 kΩ / 150 pF unpowered according to ISO10605.2008<br>• 2.0 kΩ / 330 pF powered according to ISO10605.2008 | | <br>±2000<br>±8000<br>±200<br>±500(±750)<br><br>10<br>10<br><br>10<br>8.0 | V<br><br><br><br><br>kV | (2) |

Notes

2. ESD testing is performed in accordance with the Human Body Model (HBM) ($C_{ZAP}$ = 100 pF, $R_{ZAP}$ = 1500 Ω), the Machine Model (MM) ($C_{ZAP}$ = 200 pF, $R_{ZAP}$ = 0 Ω), and the Charge Device Model.

## 4.2 Thermal characteristics

**Table 4. Thermal ratings**

| Symbol | Description (rating) | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| **Thermal ratings** | | | | | | |
| $T_A$<br>$T_J$ | Operating Temperature<br>• Ambient<br>• Junction | <br>-40<br>-40 | | <br>125<br>150 | °C | |
| $T_{STG}$ | Storage Temperature | -55 | | 150 | °C | |
| $T_{PPRT}$ | Peak Package Reflow Temperature During Reflow | – | | – | °C | |
| **Thermal resistance and package dissipation ratings** | | | | | | |
| $R_{\theta JA}$ | Junction-to-Ambient, Natural Convection, Single-layer Board | – | | 140 | °C/W | |
| $T_{SD}$ | Thermal Shutdown | | 185 | – | °C | |
| $T_{SDH}$ | Thermal Shutdown Hysteresis | – | 10 | | °C | |

## 4.3 Electrical characteristics

### 4.3.1 Static electrical characteristics

**Table 5. Static electrical characteristics**

Characteristics noted under conditions 4.5 V ≤ $V_{DD}$ ≤ 5.5 V, 2.8 V ≤ $V_{IO}$ ≤ 5.5 V, -40 °C ≤ $T_A$ ≤ 125 °C, GND = 0.0 V, R on CANx bus ($R_L$) = 60 Ω, unless otherwise noted. Typical values noted reflect the approximate parameter at $T_A$ = 25 °C under nominal conditions, unless otherwise noted.

| Symbol | Characteristic | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| **Power input VDD** | | | | | | |
| $V_{DD}$ | VDD Supply Voltage Range<br>• Nominal operation | 4.5 | – | 5.5 | V | |
| $V_{DD\_UV}$ | VDD Undervoltage Threshold | | – | 4.5 | V | |
| $I_{VDD}$ | VDD Supply Current<br>• Normal mode, TXD1 and TXD2 High<br>• Normal mode, TXD1 and TXD2 Low<br>• Standby mode | <br>–<br>–<br>– | <br>–<br>80<br>– | <br>8.0<br>130<br>10 | <br>mA<br>mA<br>µA | (3) |
| **Power input VIO** | | | | | | |
| $V_{IO}$ | VIO Supply Voltage Range<br>• Nominal operation | 2.8 | – | 5.5 | V | |
| $V_{IO\_UV}$ | VIO Undervoltage threshold | – | – | 2.8 | V | |
| $I_{VIO}$ | VIO Supply Current<br>• Normal Mode (TXD1/TXD2 high CAN1/2 bus in recessive state)<br>• Normal Mode (TXD1, TXD2 high, CAN1/2 bus in dominant state)<br>• Standby mode (STB1 and STB2 high, BUS in recessive state, wake-up filter and wake-up time out not active)<br>• Standby mode (STB1 and STB2 high, BUS in recessive state, wake- up filter and wake-up time out active) | <br>–<br>–<br>–<br>– | <br>–<br>–<br>5<br>– | <br>400<br>2.0<br>20<br>300 | <br>µA<br>mA<br>µA<br>µA | |

**Table 5. Static electrical characteristics (continued)**

Characteristics noted under conditions 4.5 V ≤ $V_{DD}$ ≤ 5.5 V, 2.8 V ≤ $V_{IO}$ ≤ 5.5 V, -40 °C ≤ $T_A$ ≤ 125 °C, GND = 0.0 V, R on CANx bus ($R_L$) = 60 Ω, unless otherwise noted. Typical values noted reflect the approximate parameter at $T_A$ = 25 °C under nominal conditions, unless otherwise noted.

| Symbol | Characteristic | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| **STB1 INPUT** | | | | | | |
| $V_{STB1}$ | Input Voltages<br>• High level input voltage<br>• Low level input voltage<br>• Input threshold hysteresis | <br>0.7 x $V_{IO}$<br>–<br>200 | <br>–<br>–<br>– | <br>–<br>0.3<br>– | <br>V<br>V<br>mV | |
| $R_{PU-STB1}$ | Pull-up resistor to $V_{IO}$ | – | 100 | – | kΩ | |
| **TXD1 INPUT** | | | | | | |
| $V_{TXD1}$ | Input Voltages<br>• High level input voltage<br>• Low level input voltage<br>• Input threshold hysteresis | <br>0.7 x $V_{IO}$<br>–<br>200 | <br>–<br>–<br>300 | <br>–<br>0.3<br>– | <br>V<br>V<br>mV | |
| $R_{PU-TXD1}$ | Pull-up Resistor to $V_{IO}$ | 5.0 | – | 50 | kΩ | |
| **RXD1 OUTPUT** | | | | | | |
| $I_{RXD1}$ | Output Current<br>• RXD1 high, VRXD1 high = $V_{IO}$ - 0.4 V<br>• RXD1 low, VRXD1 high = 0.4 V | <br>-5.0<br>1.0 | <br>-2.5<br>2.5 | <br>-1.0<br>5.0 | mA | |
| $R_{PU-RXD1}$ | Pull-up Resistor to $V_{IO}$ (in Standby mode, without toggling - no wake-up report) | 25 | 50 | 90 | kΩ | |

Notes

3. $I_{VDD}$ for CAN1 or CAN2 operation

**CANL1 and CANH1 pins**

| | | | | | | |
|---|---|---|---|---|---|---|
| $V_{REC1}$ | Recessive Voltage, TXD1 high, no load<br>• CANL1 recessive voltage<br>• CANH1 recessive voltage | <br>2.0<br>2.0 | <br>2.5<br>2.5 | <br>3.0<br>3.0 | V | |
| $V_{DIFF\_REC1}$ | CANH1 - CANL1 Differential Recessive Voltage, TXD1 high, no load | -50 | – | 50 | mV | |
| $V_{REC\_SM1}$ | Recessive voltage, sleep mode, no load<br>• CANL1 recessive voltage<br>• CANH1 recessive voltage | <br>-0.1<br>-0.1 | <br>– | <br>0.1<br>0.1 | V | |
| $V_{DOM1}$ | Dominant Voltage, TXD1 low (t < $TX_{DOM}$), $R_L$ = 45 to 65 Ω<br>• CANL1 dominant voltage<br>• CANH1 dominant voltage | <br>0.5<br>2.75 | <br>–<br>– | <br>2.25<br>4.5 | V | |
| $V_{DIFF\_DOM1}$ | CANH1 - CANL1 Differential Dominant Voltage, $R_L$ = 45 to 65 Ω, $TxD1_{LOW}$ | 1.5 | 2.0 | 3.0 | V | |
| $V_{SYM1}$ | Driver symmetry CANH1 + CANL1 | 0.9 | 1.0 | 1.1 | $V_{DD}$ | |
| $I_{LIM1}$ | Current limitation, TXD1 low (t < $TX_{DOM}$)<br>• CANL1 current limitation, CANL1 5.0 V to 28 V<br>• CANH1 current limitation, CANH1 = 0 V | <br>40<br>-100 | <br>–<br>– | <br>100<br>-40 | mA | |
| $V_{DIFF\_THR1}$ | CANH1 - CANL1 Differential Input Threshold | 0.5 | – | 0.9 | V | |
| $V_{DIFF\_HYS1}$ | CANH1 - CANL1 Differential Input Voltage Hysteresis | 50 | – | 400 | mV | |
| $V_{DIFF\_THR\_S1}$ | CANH1 - CANL1 Differential Input Threshold, in Standby mode | 0.4 | – | 1.15 | V | |
| $V_{CM1}$ | Common Mode Voltage | -15 | – | 20 | V | |
| $R_{IN1}$ | Input Resistance<br>• CANL1 input resistance<br>• CANH1 input resistance | <br>5.0<br>5.0 | <br>–<br>– | <br>50<br>50 | kΩ | |
| $R_{IN\_DIFF1}$ | CANH1, CANL1 Differential Input Resistance | 10 | – | 100 | kΩ | |

**Table 5. Static electrical characteristics (continued)**

Characteristics noted under conditions 4.5 V ≤ $V_{DD}$ ≤ 5.5 V, 2.8 V ≤ $V_{IO}$ ≤ 5.5 V, -40 °C ≤ $T_A$ ≤ 125 °C, GND = 0.0 V, R on CANx bus ($R_L$) = 60 Ω, unless otherwise noted. Typical values noted reflect the approximate parameter at $T_A$ = 25 °C under nominal conditions, unless otherwise noted.

| Symbol | Characteristic | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $R_{IN\_MATCH1}$ | Input Resistance Matching | -3.0 | – | 3.0 | % | |
| $I_{IN\_UPWR1}$ | CANL1 or CANH1 input current, device unpowered, VDD = VIO = 0 V , VCANL1 and VCANH1 0.0 to 5.0 V range<br>• VDD connected with R=0.0 KΩ to GND<br>• VDD connected with R=47 KΩ to GND | <br>-10<br>-10 | – | <br>10<br>10 | µA | |
| $R_{IN\_UPWR1}$ | CANL1, CANH1 Input Resistance, $V_{CANL1}$ = $V_{CANH1}$ = ±12 V | 10 | – | – | kΩ | |
| $C_{CAN\_CAP1}$ | CANL1, CANH1 Input Capacitance | – | 20 | – | pF | (4) |
| $C_{DIF\_CAP1}$ | CANL1, CANH1 Differential Input Capacitance | – | 10 | – | pF | (4) |
| **STB2 input** | | | | | | |
| $V_{STB2}$ | Input Voltages<br>• High level Input voltage<br>• Low level input voltage<br>• Input threshold hysteresis | <br>0.7 x $V_{IO}$<br>–<br>200 | <br>–<br>–<br>– | <br>–<br>0.3<br>– | <br>V<br>V<br>mV | |
| $R_{PU-STB2}$ | Pull-up Resistor to $V_{IO}$ | – | 100 | – | kΩ | |
| **TXD2 INPUT** | | | | | | |
| $V_{TXD2}$ | Input Voltages<br>• High level Input voltage<br>• Low level input voltage<br>• Input threshold hysteresis | <br>0.7 x $V_{IO}$<br>–<br>200 | <br>–<br>–<br>300 | <br>–<br>0.3<br>– | <br>V<br>V<br>mV | |
| $R_{PU-TXD2}$ | Pull-up Resistor to $V_{IO}$ | 5.0 | – | 50 | kΩ | |
| **RXD2 OUTPUT** | | | | | | |
| $I_{RXD2}$ | Output Current<br>• RXD2 high, VRXD2 high = $V_{IO}$ - 0.4 V<br>• RXD2 low, VRXD2 high = 0.4 V | <br>-5.0<br>1.0 | <br>-2.5<br>2.5 | <br>-1.0<br>5.0 | mA | |
| $R_{PU-RXD2}$ | Pull-up Resistor to $V_{IO}$ (in Standby mode, without toggling - no wake-up report) | 25 | 50 | 90 | kΩ | |
| **CANL2 and CANH2 Pins** | | | | | | |
| $V_{REC2}$ | Recessive Voltage, TXD2 high, no load<br>• CANL2 recessive voltage<br>• CANH2 recessive voltage | <br>2.0<br>2.0 | <br>2.5<br>2.5 | <br>3.0<br>3.0 | V | |
| $V_{DIFF\_REC2}$ | CANH2 - CANL2 Differential Recessive Voltage, TXD2 high, no load | -50 | – | 50 | mV | |
| $V_{REC\_SM2}$ | Recessive voltage, sleep mode, no load<br>• CANL2 recessive voltage<br>• CANH2 recessive voltage | <br>-0.1<br>-0.1 | <br>–<br>– | <br>1.0<br>1.0 | V | |
| $V_{DOM2}$ | Dominant Voltage, TXD2 low (t < $TX_{DOM}$), $R_L$ = 45 Ω to 65 Ω<br>• CANL2 dominant voltage<br>• CANH2 dominant voltage | <br>0.5<br>2.75 | <br>–<br>– | <br>2.25<br>4.5 | V | |
| $V_{DIFF\_DOM2}$ | CANH2 - CANL2 Differential Dominant Voltage, $R_L$ = 45 Ω to 65 Ω, $TxD2_{LOW}$ | 1.5 | 2.0 | 3.0 | V | |
| $V_{SYM2}$ | Driver symmetry CANH2 + CANL2 | 0.9 | 1.0 | 1.1 | $V_{DD}$ | |
| $I_{LIM2}$ | Current Limitation, TXD2 low (t < $TX_{DOM}$)<br>• CANL2 current limitation, CANL2 5.0 V to 28 V<br>• CANH2 current limitation, CANH2 = 0.0 V | <br>40<br>-100 | <br>–<br>– | <br>100<br>-40 | mA | |

Notes

4. Guaranteed by design and characterization

**Table 5. Static electrical characteristics (continued)**

Characteristics noted under conditions 4.5 V ≤ $V_{DD}$ ≤ 5.5 V, 2.8 V ≤ $V_{IO}$ ≤ 5.5 V, -40 °C ≤ $T_A$ ≤ 125 °C, GND = 0.0 V, R on CANx bus ($R_L$) = 60 Ω, unless otherwise noted. Typical values noted reflect the approximate parameter at $T_A$ = 25 °C under nominal conditions, unless otherwise noted.

| Symbol | Characteristic | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| **CANL2 and CANH2 Pins (continued)** | | | | | | |
| $V_{DIFF\_THR2}$ | CANH2 - CANL2 Differential Input Threshold | 0.5 | – | 0.9 | V | |
| $V_{DIFF\_HYS2}$ | CANH2 - CANL2 Differential Input Voltage Hysteresis | 50 | – | 400 | mV | |
| $V_{DIFF\_THR\_S2}$ | CANH2 - CANL2 Differential Input Threshold, in Standby mode | 0.4 | – | 1.15 | V | |
| $V_{CM2}$ | Common Mode Voltage | -15 | – | 20 | V | |
| $R_{IN2}$ | Input Resistance<br>• CANL2 input resistance<br>• CANH2 input resistance | <br>5.0<br>5.0 | <br>–<br>– | <br>50<br>50 | kΩ | |
| $R_{IN\_DIFF2}$ | CANH2, CANL2 Differential Input Resistance | 10 | – | 100 | kΩ | |
| $R_{IN\_MATCH2}$ | Input Resistance Matching | -3.0 | – | 3.0 | % | |
| $I_{IN\_UPWR2}$ | CANL2 or CANH2 input current, device unpowered, VDD = VIO = 0 V , VCANL2 and VCANH2 0.0 to 5.0 V range<br>• VDD connected with R=0KOhm to GND<br>• VDD connected with R=47KOhm to GND | <br>-10<br>-10 | <br>–<br>– | <br>10<br>10 | µA | |
| $R_{IN\_UPWR2}$ | CANL2, CANH2 Input Resistance, VCANL2 = VCANH2= ±12 V | 10 | – | – | kΩ | |
| $C_{CAN\_CAP2}$ | CANL2, CANH2 Input Capacitance (guaranteed by design and characterization) | – | 20 | – | pF | |
| $C_{DIF\_CAP2}$ | CANL2, CANH2 Differential Input Capacitance | – | 10 | – | pF | (5) |
| $T_{SD}$ | Thermal Shutdown | 150 | 185 | – | °C | |

Notes

5. Guaranteed by design and characterization

## 4.3.2 Dynamic electrical characteristic

**Table 6. Dynamic electrical characteristics**

Characteristics noted under conditions 4.5 V ≤ $V_{DD}$ ≤ 5.5 V, 2.8 V ≤ $V_{IO}$ ≤ 5.5 V, -40 °C ≤ $T_A$ ≤ 125 °C, GND = 0 V, R on CANx bus ($R_L$) = 60 Ω, unless otherwise noted. Typical values noted reflect the approximate parameter at $T_A$ = 25 °C under nominal conditions, unless otherwise noted.

| Symbol | Characteristic | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| **Timing parameterS** | | | | | | |
| $tX_{DOM}$ | TXD DOM | 2.5 | – | 16 | ms | (6) |
| $t_{LOOP}$ | T Loop | – | – | 255 | ns | |
| $t_{WU\_FLT1}$ | TWU Filter1 | 0.5 | – | 5.0 | µs | |
| $t_{WU\_FLT2}$ | TWU Filter2 | 0.08 | – | 1.0 | µs | |
| $t_{TGLT}$ | Tdelay During Toggling | – | – | 1.5 | µs | |
| $t_{WU\_TO}$ | Twake-up Timeout | 1.5 | – | 7.0 | ms | |
| $t_{DELAY\_PWR}$ | Delay Between Power-up and Device Ready | – | 120 | 300 | µs | |
| $t_{DELAY\_SN}$ | Transition Time from Standby to Normal mode (STB high to low) | – | – | 40 | µs | |

Notes

6. 33CM0902 version only

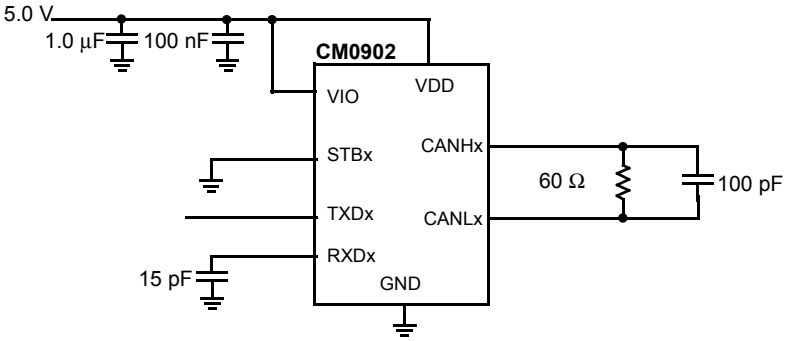



**Figure 3. Timing test circuit**

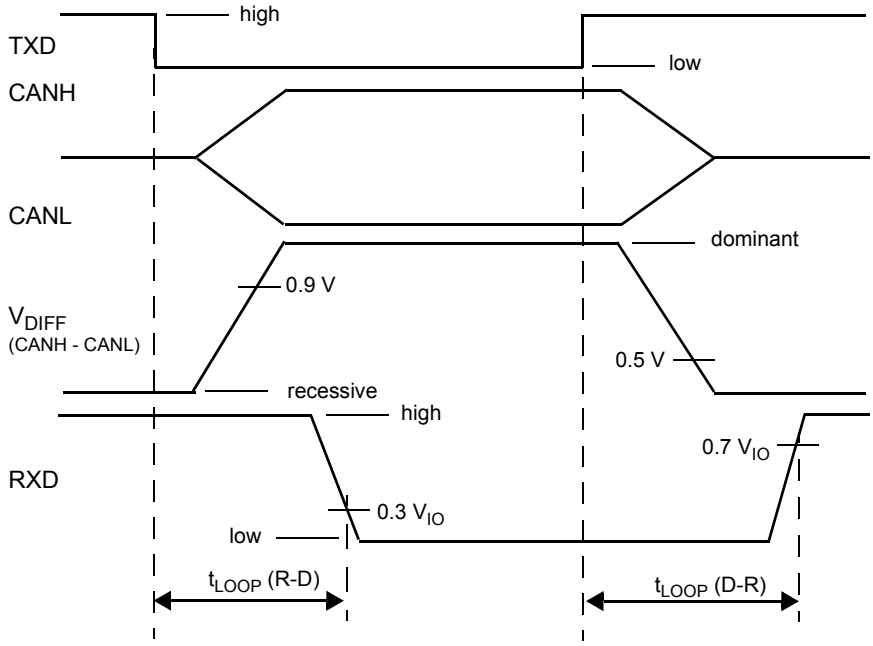



**Figure 4. CAN timing diagram**

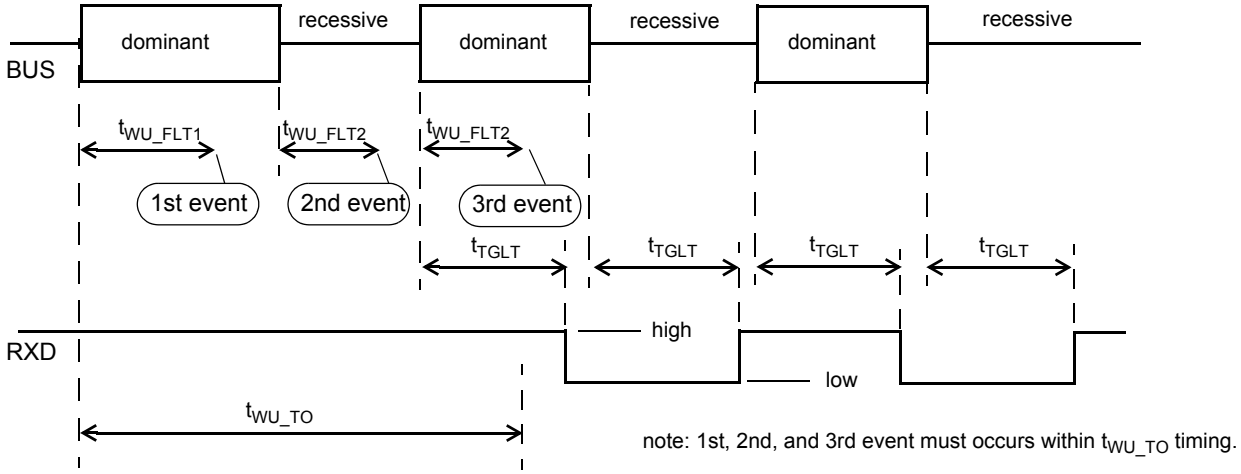



**Figure 5. Wake-up pattern timing illustration**

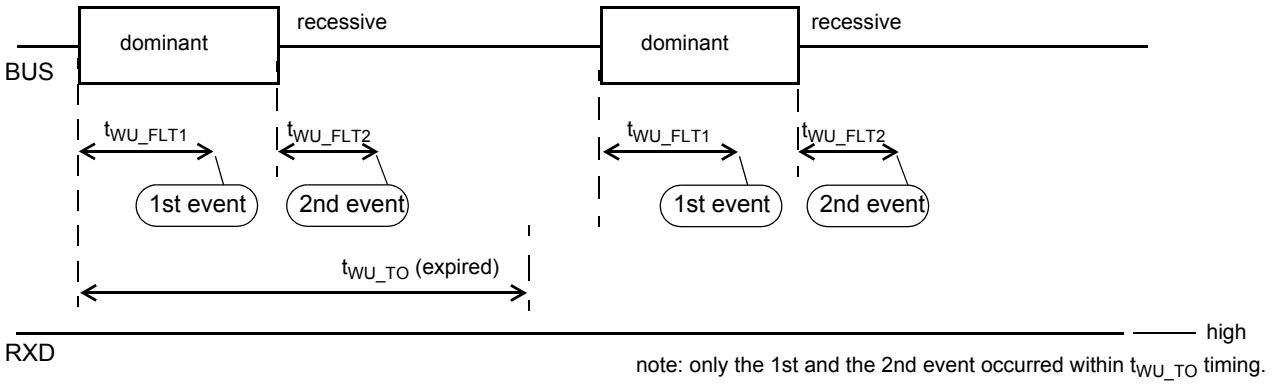



**Figure 6. Timeout wake-up timing illustration**

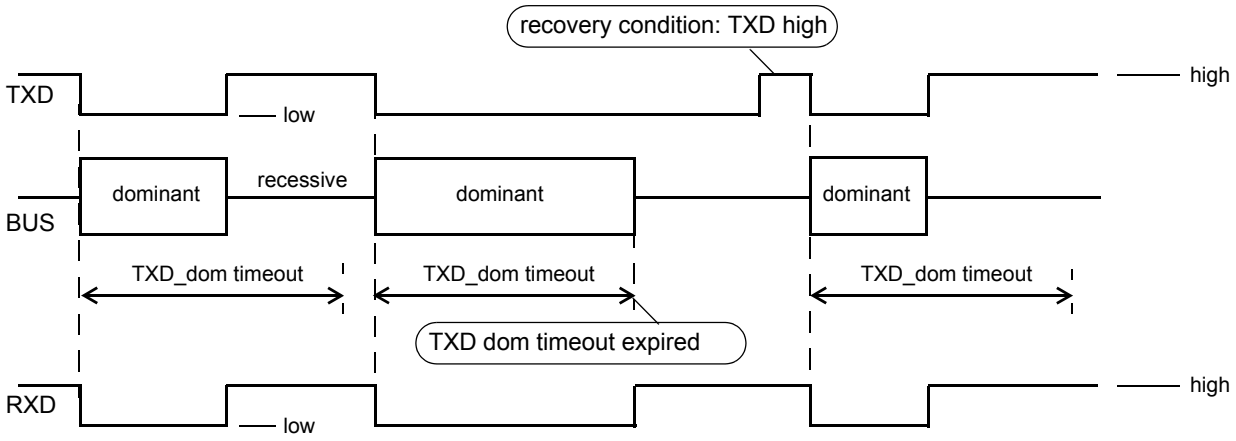



**Figure 7. TXD dominant timeout detection illustration**

## 4.4 Operating conditions

This section describes the operating conditions of the device. Conditions apply to all the following data, unless otherwise noted.

**Table 7. Operating conditions**

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

| Symbol | Ratings | Min. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| $V_{DD\_F}$ | Functional Operating $V_{DD}$ voltage | $V_{DD\_UV}$ | 7.0 | V | (7) |
| $V_{DD\_OP}$ | Parametric Operating $V_{DD}$ voltage | 4.5 | 5.5 | V | |
| $V_{IO\_F}$ | Functional Operating $V_{IO}$ voltage | $V_{IO\_UV}$ | 7.0 | V | (7) |
| $V_{IO\_OP}$ | Parametric Operating $V_{IO}$ voltage | 2.8 | 5.5 | V | |

Notes

7. Functional operating voltage is defined as device functional or CAN in recessive state

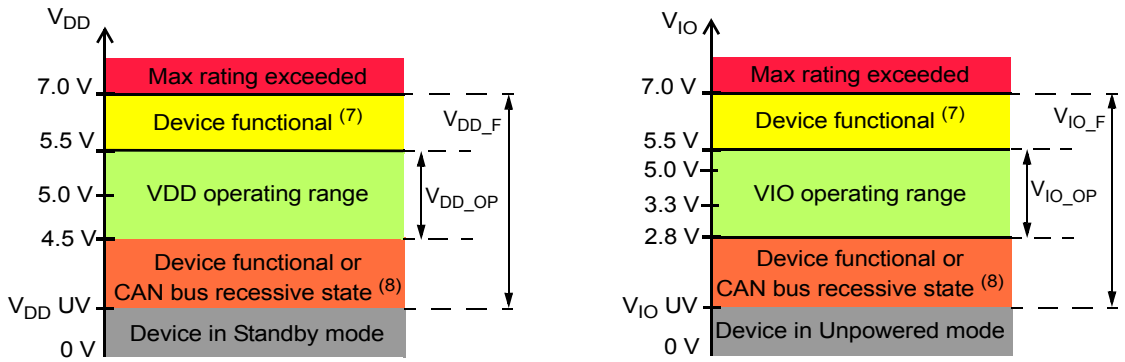



**Figure 8. Supply voltage operating range**

Notes

8. **Device functional**: Device can operate in this voltage range without damage. Electrical characteristics are not fully guaranteed in this range.
9. **Device functional or CAN bus recessive state**: Device is either functional (see Note 1), or is maintained in recessive state. No false dominant state on CAN bus; dominant state is only controlled by TXDx low level.

# 5 General IC functional description and application information

The CM0902 is a SMARTMOS two channel high-speed CAN transceiver, providing the physical interface between the CAN protocol controller of an MCU and the physical two-wire CAN bus, featuring CAN bus wake-up on each CAN channel and TXD dominant timeout (33CM0902 version only). The two CAN physical layers are packaged in a 14-pin SOIC with market standard pin out, and offer excellent EMC and ESD performance without the need for external filter components. These meet the ISO 11898-2 and ISO11898-5 standards, and provide low leakage on CAN bus while unpowered.

The device is supplied from VDD, while VIO allows automatic operation with 5.0 V and 3.3 V microcontrollers interface.

## 5.1 Features

- Very low current consumption in standby mode
- Automatic adaptation to 3.3 V or 5.0 V MCU communication
- Standby mode with remote CAN wake-up
- Pin and function compatible with market standard
- Cost efficient robustness:
  - High system level ESD performance
  - Very high electromagnetic Immunity and low electromagnetic emission without common mode choke or other external components.
- Fail-safe behaviors:
  - TXD Dominant timeout (33CM0902 only)
  - Ideal passive behavior when unpowered, CAN bus leakage current <10 μA.
- $V_{DD}$ and $V_{IO}$ monitoring

## 5.2 Functional Block Diagram

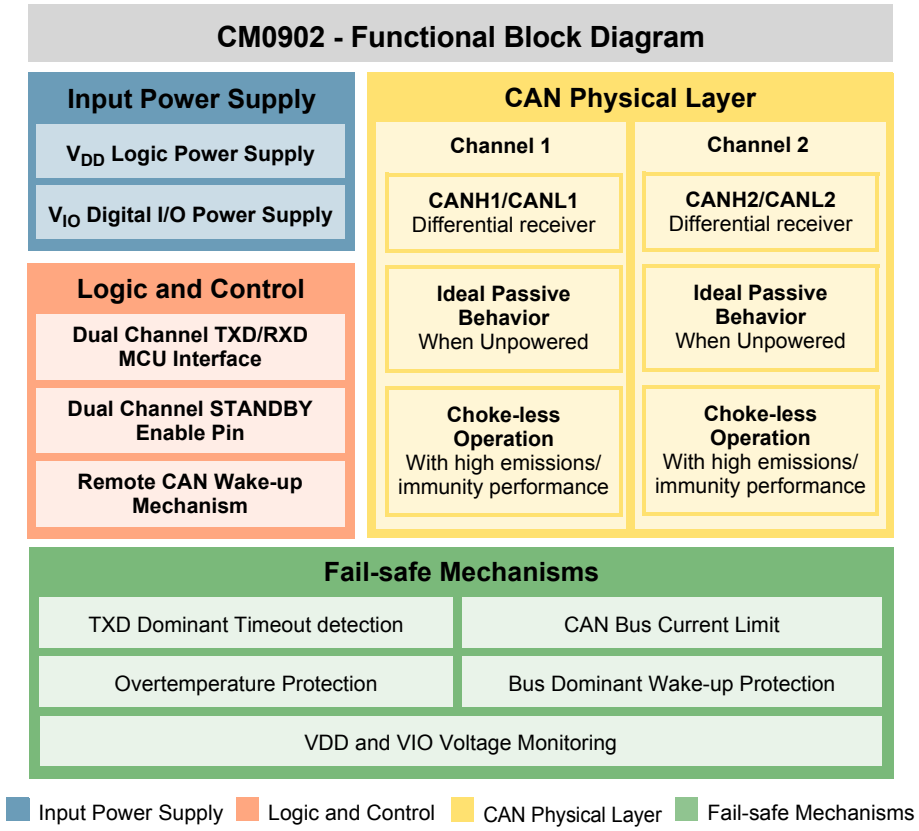



**Figure 9. Functional block diagram**

## 5.3 Functional description

### 5.3.1 $V_{DD}$ power supply

This is the supply for the CANHx and CANLx bus drivers, the bus differential receiver and the bus biasing voltage circuitry. $V_{DD}$ is monitored for undervoltage conditions. See Fail-safe mechanisms.

When the device is in standby mode, the consumption on VDD is extremely low (Refer to IVDD).

### 5.3.2 $V_{IO}$ digital I/O power supply

This is the supply for the TXDx, RXDx, and STBx digital input outputs pins. $V_{IO}$ also supplies the low power differential wake-up receivers and filter circuitry. This allows detecting and reporting bus wake-up events with device supplied only from $V_{IO}$. $V_{IO}$ is monitored for undervoltage conditions. See Fail-safe mechanisms.

When the device is in Standby mode, the consumption on $V_{IO}$ is extremely low (Refer to IVIO).

### 5.3.3 STB1 and STB2

STBx are the input pins to control the CANx interface mode. When STBx is high or floating, the respective CANx interface is in Standby mode. When STBx is low, the CANx interface is set in Normal mode. STBx has an internal pull-up to the VIO pin, so if STBx is left open, the CANx is set to the predetermined Standby mode.

### 5.3.4 TXD1 and TXD2

TXDx is the device input pin to control the CANx bus level. In the application, this pin is connected to one of the microcontroller's transmit pins. When TXDx is high or floating, the CANHx and CANLx drivers are OFF in Normal mode, setting the bus in a recessive state. When TXDx is low, the CANHx and CANLx drivers are activated and the bus is set to a dominant state. TXDx has a built-in timing protection on the 33CM0902 version, which disables the bus when TXDx is dominant for more than $tX_{DOM}$.

In Standby mode, TXDx has no effect on the respective CANx interface.

### 5.3.5 RXD1 and RXD2

RXDx is the bus output level report pin. This pin connects to one of the microcontroller's receive pins in the application. RXDx is a push-pull structure in Normal mode. When the respective CANx bus is in a recessive state, RXDx is high, and low when the bus is dominant.

In Standby mode, the push-pull structure is disabled, RXDx is pulled up to VIO via a resistor ($R_{PU-RXD1}$), and is in a high level. When the bus wake-up is detected, the push-pull structure resumes and RXDx reports a wake-up via a toggling mechanism (refer to Figure 5).

### 5.3.6 CANH1 / CANL1 and CANH2 / CANL2

These are the CAN bus pins and each channel 1 or 2 is fully independent from each other. CANLx is a low-side driver to GND, and CANHx is a high-side driver to VDD. In Normal mode and TXDx high, the CANHx and CANLx drivers are OFF, and the voltage at CANHx and CANLx is approx. 2.5 V, provided by the internal bus biasing circuitry. When TXDx is low, CANLx is pulled to GND and CANHx to VDD, creating a differential voltage on the CAN bus.

CANHx and CANLx drivers are OFF in Standby mode, and pulled to GND via the CANx interface $R_{IN}$ resistors (ref to parameter Input Resistance). CANHx and CANLx are high-impedance with extremely low leakage to GND in device unpowered mode, making the device ideally passive when unpowered. CANHx and CANLx have integrated ESD protection and extremely high robustness versus external disturbance, such as EMC and electrical transients. These pins have current limitation and thermal protection.

# 6 Functional operation

## 6.1 Operating modes

The CM0902 provides two CAN, each one capable of independently operating in two modes: Standby and Normal.

### 6.1.1 Normal mode

This mode is selected when the STBx pin is low. In this mode, the device is able to transmit information from TXDx to the bus and report the bus level on the RXDx pin. When TXDx is high, CANHx and CANLx drivers are off and the bus is in the recessive state (unless it is in an application where another device drives the bus to the dominant state). When TXDx is low, CANHx and CANLx drivers are ON and the bus is in the dominant state.

### 6.1.2 Standby mode

This mode is selected when the STBx pin is high or floating. The device is not able to transmit information from TXDx to the bus and it cannot report accurate bus information in this mode. The device can only report bus wake-up events via the RXDx toggling mechanism.

When both CAN interfaces are in Standby mode, the power consumption from $V_{DD}$ and $V_{IO}$ is extremely low. The CANHx and CANLx pins are pulled to GND via the internal $R_{IN}$ resistors in this mode.

#### 6.1.2.1 Wake-up mechanism

The CM0902 includes bus monitoring circuitry to detect and report bus wake-ups. To activate a wake-up report, three events must occur on the CAN bus:

- event 1: a dominant level for a time longer than $t_{WU\_FLT1}$ followed by
- event 2: a recessive level (event 2) longer than $t_{WU\_FLT2}$ followed by
- event 3: a dominant level (event 3) longer than $t_{WU\_FLT2}$.

The RXD pin reports the bus state (bus dominant => RXD low, bus recessive => RXD high). The delay between bus dominant and RXD low, and bus recessive and RXD high is longer than in Normal mode (refer to $t_{TGLT}$). The three events must occur within the $t_{WU\_TO}$ timeout.

Figure 5 “Wake-up pattern timing illustration” illustrates the wake-up detection and reporting (toggling) mechanism.

If the three events do not occur within the $T_{WU\_TO}$ timeout, the wake-up and toggling mechanism are not activated. This is illustrated in Figure 6. The three events and the timeout function avoid a permanent dominant state on the bus which would generate a permanent wake-up situation, and prevent the system from entering into Low-power mode.

### 6.1.3 Unpowered mode

When $V_{IO}$ is below $V_{IO\ UV}$, the device is in unpowered mode. Both CAN buses is in high-impedance and not able to transmit, receive, or report bus wake-up events through any of the buses.

## 6.2 Fail-safe mechanisms

The device implements various protection, detection, and predictable fail-safe mechanisms explained below.

### 6.2.1 STB and TXD input pins

The STBx input pin has an internal integrated pull-up structure to the VIO supply pin. If STBx is open, the respective CANx interface is set to Standby mode to ensure predictable behavior and minimize system current consumption.

The TXDx input pin also has an internal integrated pull-up structure to the VIO supply pin. If TXDx is open, the CANx driver is set to the recessive state to minimize current consumption and ensure no false dominant bit is transmitted on the bus.

## 6.2.2 TXD dominant timeout detection

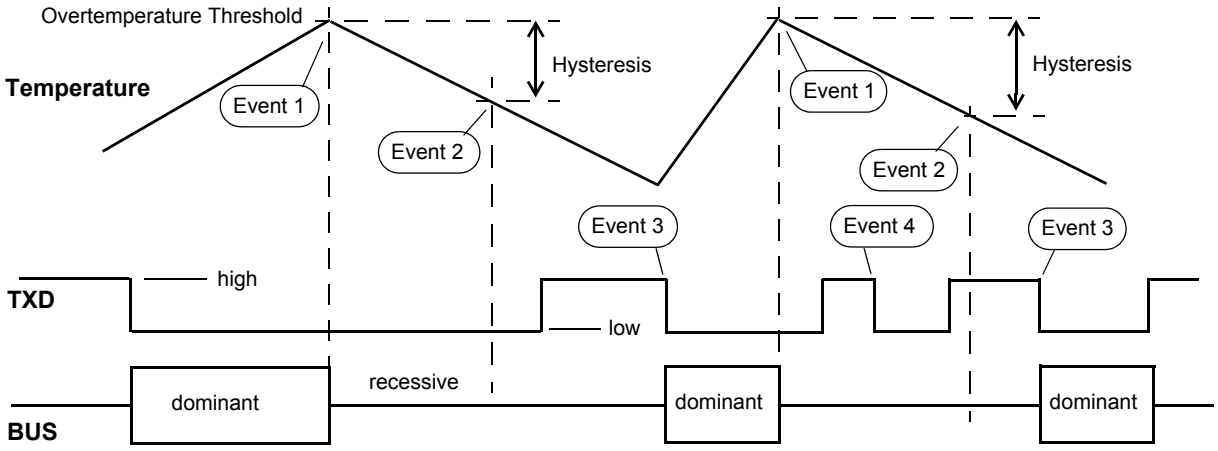
The 33CM0902 device implements a TXD dominant timeout detection and protection mechanism. If TXDx is set low for a time longer than the $tX_{DOM}$ parameter, the CANx drivers are disabled and the CANx bus returns to the recessive state. This prevents the bus from being set to the dominant state permanently in case a fault sets the TXDx input to low level permanently. The device recovers when a high level is detected on TXDx (Refer to Figure 7).

## 6.2.3 CAN current limitation

The current flowing in and out of the CANHx and CANLx driver is limited to a maximum of 100 mA, in case of a short-circuit (parameter for $I_{LIM1}$).

## 6.2.4 CAN overtemperature

If the driver temperature exceeds $T_{SD}$, the driver turns off to protect the device. A hysteresis is implemented in this protection feature. The device overtemperature and recovery conditions are shown in Figure 10. The driver remains disabled until the temperature has fallen below the OT threshold minus the hysteresis and a TXD high to low transition is detected. Since both CAN interfaces are fully independent, each driver requires a high to low transition of its own TXDx pin to re-enable the CAN driver.




Event 1: overtemperature detection. CAN driver disabled.
Event 2: temperature falls below “overtemperature. threshold minus hysteresis” => CAN driver remains disabled.
Event 3: temperature below “overtemperature. threshold minus hysteresis” and TxD high to low transition => CAN driver enabled.
Event 4: temperature above “overtemperature. threshold minus hysteresis” and TxD high to low transition => CAN driver remains disabled.

**Figure 10. Overtemperature behavior**

## 6.2.5 $V_{DD}$ and $V_{IO}$ supply voltage monitoring

The device monitors the $V_{DD}$ and $V_{IO}$ supply inputs.

The device is set in Standby mode if $V_{DD}$ falls below $V_{DD\ UV}$ (VDD_UV). This ensures a predictable behavior due to the loss of $V_{DD}$. CAN drivers, receiver, or bus biasing cannot operate any longer. In this case, the bus wake-up is available as $V_{IO}$ remains active.

If $V_{IO}$ falls below $V_{IO\ UV}$ (VIO_UV), the device is set to an unpowered condition. This ensures a predictable behavior due to the loss of $V_{IO}$, CAN drivers, receivers, or bus biasing cannot operate any longer. This sets the bus in high-impedance and in ideal passive condition.

## 6.2.6 Bus dominant state behavior in standby mode

When the CAN interface is in Standby mode, a bus dominant condition due to a short-circuit or a fault in any of the CAN nodes, does not generate a permanent wake-up event, since the specific wake-up sequence and timeout protect the device from waking-up with an unwanted event.

## 6.3 Device operation summary

The following table summarizes the CAN interface operation and the state of the input/output pins, depending on the operating mode and power supply conditions.

**Standby and normal modes**

| mode | Description | $V_{DD}$ range | $V_{IO}$ range | STBx | TXDx | RXDx | CANx | Wake-up |
|---|---|---|---|---|---|---|---|---|
| Normal | Nominal supply and normal mode | from 4.5 V to 5.5 V | from 2.8 V to 5.5 V | Low | TXD High => bus recessive TXD Low => bus dominant | Report CAN state (bus recessive => RXD high, bus dominant => RXD low). | CANH and CANL drivers controlled by TXD input.<br>Differential receiver reports the bus state on RXD pin.<br>Biasing circuitry provides approx 2.5 V in recessive state. | Disabled |
| Standby | Nominal supply and standby mode | from 0.0 V to 5.5 V | from 2.8 V to 5.5 V | High or floating | No effect. on CAN bus. | Report bus wake up via toggling mechanism. | CAN driver and differential receiver disabled.<br>Bus biased to GND via internal $R_{IN}$ resistors. | Enabled |

**Undervoltage and loss of power conditions**

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Standby due to $V_{DD}$ loss | Device in standby mode due to loss of $V_{DD}$ ($V_{DD}$ falls below $V_{DD\ UV}$) | from 0.0 to $V_{DD\_UV}$. (11) | from 2.8 V to 5.5 V (12) | X (10) | X | Report bus wake up via toggling mechanism. | CAN driver and differential receiver disabled.<br>Bus biased to GND via internal $R_{IN}$ resistors. | Enabled |
| Unpowered due to $V_{IO}$ loss | Device in unpowered state due to low $V_{IO}$. CAN bus high-impedance. | (11) | from 0.0 V to $V_{IO\_UV}$ | X | X | Pulled up to $V_{IO}$ down to $V_{IO}$ approx = 1.5 V, then released. | CAN driver and differential receiver disabled.<br>High-impedance, with ideal passive behavior. | Not available. |

Notes

10. STBx pin has no effect. CANx Interface enters in Standby mode.
11. $V_{DD}$ consumption < 10 uA down to $V_{DD}$ approx 1.5 V.
12. $V_{IO}$ consumption < 10 uA down to $V_{IO}$ approx 1.5 V. If STB is high or floating.

# 7 Typical applications

## 7.1 Application diagrams

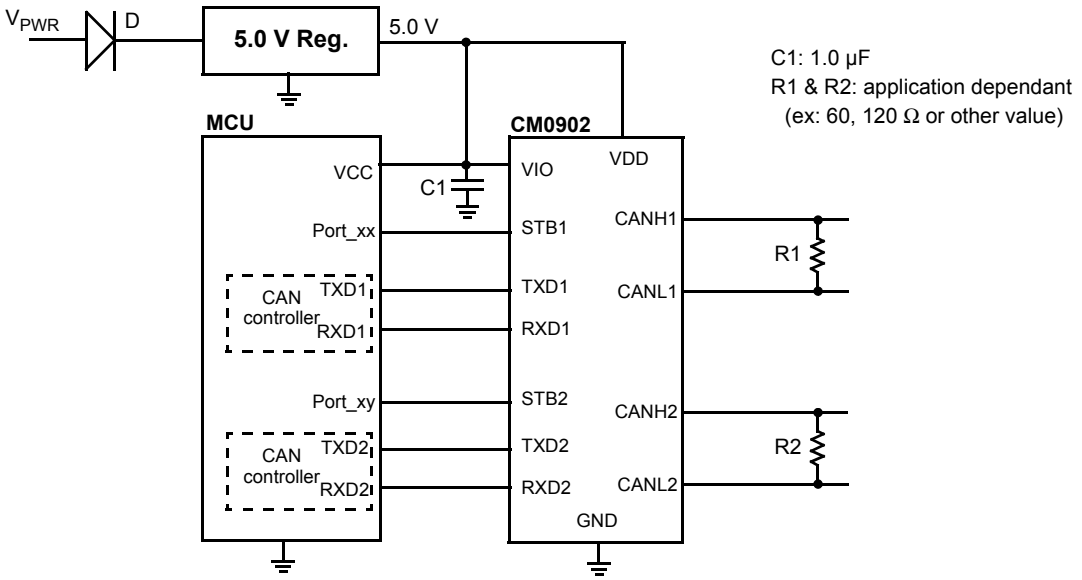



**Figure 11. Single supply typical application schematic**

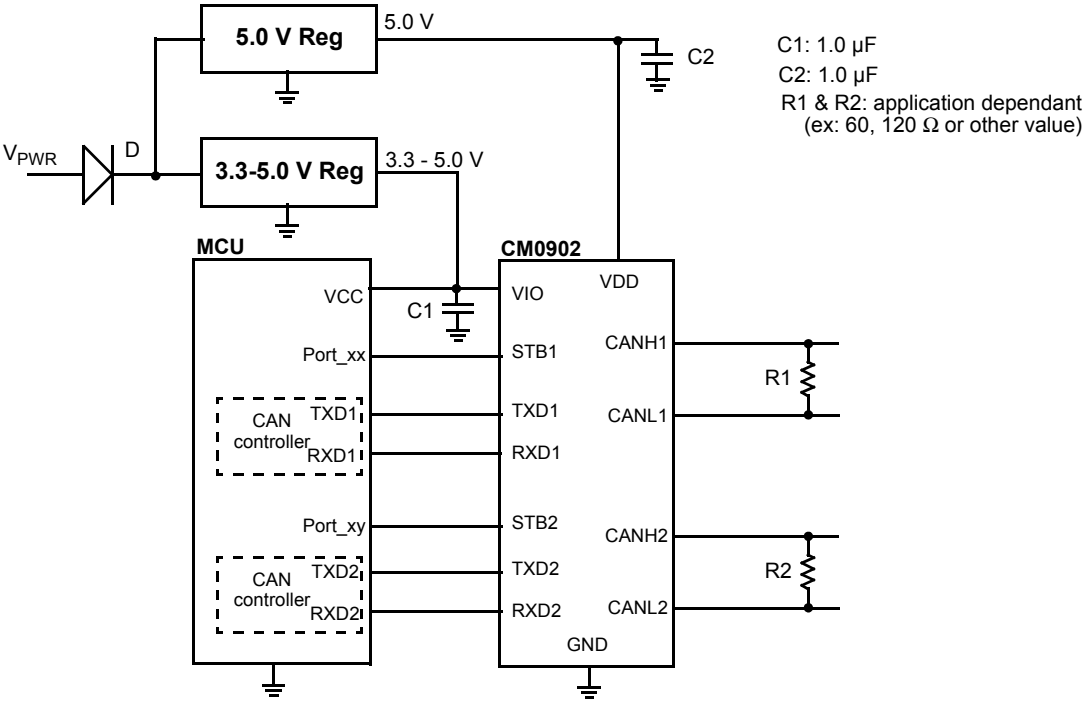
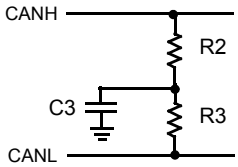



**Figure 12. Dual supply typical application schematic**




R2, R3: application dependant
(ex: 60 ohm or other value):

C3: application dependant
(ex: 4.7 nF or other value):

**Figure 13. Example of bus termination options**

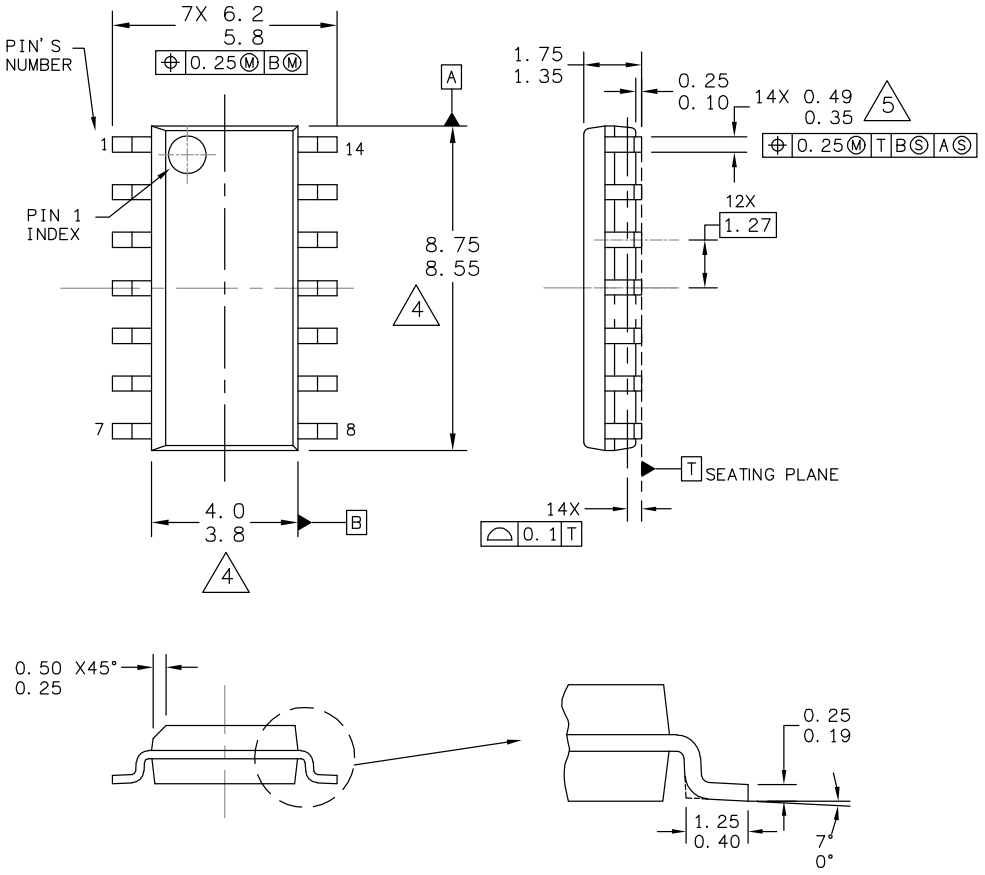
# 8 Packaging

## 8.1 Package mechanical dimensions

Package dimensions are provided in package drawings. To find the most current package outline drawing, go to www.nxp.com and perform a keyword search for the drawing's document number.

**Table 8. Packaging Information**

| Package | Suffix | Package outline drawing number |
|---|---|---|
| 14-Pin SOICN | EF | 98ASB42565B |




| © NXP SEMICONDUCTORS N.V. ALL RIGHTS RESERVED | MECHANICAL OUTLINE | PRINT VERSION NOT TO SCALE |
|---|---|---|
| TITLE: 14LD SOIC N/B, 1.27 PITCH CASE-OUTLINE | DOCUMENT NO: 98ASB42565B | REV: L |
| | STANDARD: JECDEC MS-012AB | |
| | SOT108-4 | 11 APR 2016 |

**CM0902**

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. DATUMS A AND B TO BE DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY. DATUM T IS A SURFACE.
4. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.15 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
5. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTOAL IN EXCESS OF THE LEAD WIDTH AT MAXIMUM MATERIAL CONDITION.



| MECHANICAL OUTLINE | PRINT VERSION NOT TO SCALE |
|---|---|

| TITLE: 14LD SOIC N/B, 1.27 PITCH CASE–OUTLINE | DOCUMENT NO: 98ASB42565B REV: L |
|---|---|
| | STANDARD: JECDEC MS–012AB |
| | SOT108–4 11 APR 2016 |

# 9 Revision history

| Revision | Date | Description of changes |
|---|---|---|
| 1.0 | 6/2014 | • Initial release |
| 2.0 | 11/2014 | • Data adjusted to match latest silicon |
| 3.0 | 1/2015 | • Changed ordering information from PC to MC |
| 4.0 | 4/2015 | • Added information for dual speed (up to 1 Mbit/s)<br>• Added $V_{REC\_SM1}$ & $V_{REC\_SM2}$ (CANH, CANL recessive voltage, sleep mode) to Table 5<br>• Added driver symmetry $V_{SYM1}$ & $V_{SYM2}$ to Table 5<br>• Updated $I_{IN\_UPWR1}$ & $I_{IN\_UPWR2}$ in Table 5 |
| | 8/2016 | • Updated document to NXP form and style |

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Rev. 4.0
8/2016